

WHAT IS CLAIMED IS:

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- 1 1. A method of decoding encoded image data comprising
 - 2 the steps of:
 - 3 operating a decoder circuit implemented in
 - 4 hardware to perform at least one non-memory intensive
 - 5 image decoding operation to generate, from the encoded
 - 6 image data, a first set of processed image data, the at
 - 7 least one non-memory intensive image decoding operation
 - 8 being an operation in the group of operations consisting
 - 9 of a variable length decoding operation, an inverse scan
 - 10 conversion operation, and an inverse quantization
 - 11 operation;
 - 12 supplying the first set of processed image data
 - 13 generated by the decoder circuit to a programmable
 - 14 processor; and
 - 15 operating the programmable processor to perform
 - 16 at least one additional image decoding operation using
 - 17 the first set of processed image data.

1 2. The method of claim 1, wherein the step of operating
2 the decoder circuit, includes the step of performing at
3 least two additional operations from the group of
4 operations consisting of a variable length decoding
5 operation, an inverse scan conversion operation, an
6 inverse quantization operation, an inverse discrete
7 cosine transform operation, and a data reduction
8 operation, the two additional operations being different
9 from said at least one non-memory intensive operation.

1 3. The method of claim 1, wherein the step of operating
2 the decoder circuit further includes:
3 operating the decoder circuit to perform a data reduction
4 operation.

1 4. The method of claim 2, wherein the step of operating
2 the decoder circuit further includes:
3 operating the decoder circuit to perform a data
4 reduction operation.

1 5. The method of claim 2, wherein the step of operating
2 the programmable processor to perform at least one
3 additional image decoding operation includes the step of:
4 operating the programmable processor to perform a
5 motion compensated prediction operation.

1 6. The method of claim 5, wherein the step of operating
2 the programmable processor to perform at least one
3 additional image decoding operation further includes the
4 step of:

5 operating the programmable processor to combine
6 decoded image data produced by performing the motion
7 compensated prediction operation with decoded residual
8 image data to produce a set of decoded image data
9 representing reconstructed pixels.

1 7. The method of claim 1, wherein the step of operating
2 the programmable processor to perform at least one
3 additional image decoding operation includes the step of:

4 operating the programmable processor to combine
5 decoded image data produced by performing a motion
6 compensated prediction operation with decoded intra-coded
7 image data to produce a set of decoded image data
8 representing a complete frame.

1 8. The method of claim 2, wherein the programmable
2 processor is coupled to a graphics processor, the method
3 further comprising the step of:

4 operating the graphics processor to perform a motion
5 compensated prediction operation using data included in
6 the first set of processed data.

1 9. The method of claim 8, wherein the step of operating
2 the programmable processor to perform at least one
3 additional image decoding operation further includes the
4 step of:

5 operating the programmable processor to combine
6 decoded image data produced by performing the motion
7 compensated prediction operation with decoded residual
8 image data to produce a set of decoded image data
9 representing reconstructed pixels.

1 10. The method of claim 8, further comprising the step
2 of:

3 storing in the decoder circuit multiple sets of
4 context information, each set of stored context
5 information corresponding to a different one of a
6 plurality of encoded data streams processed by the
7 decoder circuit.

1 11. The method of claim 1, further comprising the step
2 of:

3 storing in the decoder circuit multiple sets of
4 context information, each set of stored context
5 information corresponding to a different one of a
6 plurality of encoded data streams processed by the
7 decoder circuit.

1 12. The method of claim 11, further comprising the step
2 of:

3 operating the decoder circuit to access the
4 stored set of context information corresponding to an
5 encoded data stream when the data stream is to be
6 processed by the decoder circuit.

1 13. The method of claim 12, wherein each set of stored
2 context information includes encoded data stream syntax
3 information.

1 14. A method of decoding encoded image data including
2 inter-coded image data and intra-coded image data, the
3 method comprising the steps of:

4 operating an intra-coded video decoder circuit
5 implemented in hardware to decode said intra-coded image
6 data and to output prediction residual data produced from
7 said encoded image data; and

8 controlling a programmable processor to perform
9 an inter-coded decoding operation using said prediction
10 residual image data.

1 15. The decoding method of claim 14, wherein the step of
2 controlling a programmable processor to perform a
3 decoding operation includes the step of:

4 controlling the programmable processor to
5 perform a motion compensated prediction operation.

1 16. The decoding method of claim 14, wherein the step of
2 controlling a programmable processor to perform an inter-
3 coded decoding operation includes the step of:

4 operating the programmable processor to control
5 the supply of motion vector information to a graphics
6 processor.

1 17. The decoding method of claim 14, further comprising
2 the step of:

3 controlling a graphics processor coupled to said
4 programmable processor to perform a motion compensated
5 prediction operation.

1 18. The decoding method of claim 14, wherein the step of
2 operating the decoder circuit to decode said intra-coded
3 image data includes performing a complete decoding
4 operation on said intra-coded image data to produce fully
5 decoded image data therefrom.

1 19. A method of decoding encoded image data comprising
2 the steps of:

3 operating a decoder circuit implemented in
4 hardware to perform non-memory intensive image decoding
5 operations to generate, from the encoded image data, a
6 first set of processed image data, at least one of said
7 non-memory intensive image decoding operation being a
8 data reduction operation;

9 supplying the first set of processed image data
10 generated by the decoder circuit to a programmable
11 processor; and

12 operating the programmable processor to perform
13 at least one additional image decoding operation using
14 the first set of processed image data.

1 20. A system for decoding encoded image data including
2 intra-coded image data and inter-coded image data, the
3 system comprising:

4 an intra-coded data decoding circuit for decoding
5 intra-coded image data;

6 a programmable processor coupled to the intra-coded
7 data decoding circuit; and

8 a memory including a video decoding routine for
9 controlling the programmable processor to perform at
10 least one inter-coded data decoding operation.

1 21. The system of claim 20, further comprising:

2 a graphics processor coupled to the
3 programmable processor.

1 22. The system of claim 20, wherein the intra-coded data
2 decoding circuit includes:

3 an inverse discrete cosine transform circuit and an
4 inverse quantization circuit.

1 23. The system of claim 22, further comprising:

2 a motion vector reconstruction circuit for
3 reconstructing motion vectors included in said inter-
4 coded image data, the motion vector reconstruction
5 circuit being coupled to said programmable processor.

1 24. The system of claim 23, wherein said intra-coded
2 data decoding circuit and motion vector reconstruction
3 circuit are implemented on a first semiconductor chip and
4 wherein said programmable processor is implemented on a
5 second semiconductor chip.

1 25. The system of claim 23, wherein said intra-coded
2 data decoding circuit, motion vector reconstruction
3 circuit and programmable processor are implemented on a
4 single semi-conductor chip.

1 26. The system of claim 20, wherein the intra-coded data
2 decoding circuit includes a variable length decoding
3 circuit for processing both intra-coded and inter-coded
4 image data.

1 27. The system of claim 26,
2 wherein the intra-coded data decoding circuit
3 further includes an inverse discrete cosine transform
4 circuit and an inverse quantization circuit;

5 wherein the system further includes a motion
6 vector reconstruction circuit for reconstructing motion
7 vectors included in said inter-coded image data coupled
8 to said programmable processor; and

9 wherein the variable length decoding circuit includes
10 means for outputting intra-coded data to the inverse
11 quantization circuit and means for outputting motion
12 vector information to the motion vector reconstruction
13 circuit.

1 28. The system of claim 20, wherein the intra-coded data
2 decoding circuit and the programmable processor are
3 implemented on two separate semi-conductor chips.

1 29. An apparatus for processing encoded image data
2 including motion vector information, the apparatus
3 comprising:

4 a motion vector reconstruction circuit for
5 performing motion vector reconstruction operations using
6 motion vector information included in the encoded image
7 data; and

8 means for outputting to a programmable
9 processor reconstructed motion vectors generated by the
10 motion vector reconstruction circuit.

1 30. The apparatus of claim 29, further comprising:

2 said programmable processor coupled to the
3 means for outputting; and

4 a memory device coupled to said programmable
5 processor, the memory device including a video decoding
6 routine used to control said programmable processor to
7 perform a video decoding operation using reconstructed
8 motion vectors received from the means for outputting.